CLAIMS

What is claimed is:

1. An electronic audio system comprising:

a buffer communicatively coupled to a first audio processing module and a second audio processing module, for storing audio data generated by said first audio processing module and consumed by said second audio processing module;

a clock manager communicatively coupled to said first and second audio processing modules, for determining a first clock source of said first audio processing module, for determining a second clock source of said second audio processing module and for configuring said first and second audio processing modules and a sample rate converter as a function of said first clock source and said second clock source; and

said sample rate converter communicatively coupled to said buffer and said clock manager, for synchronizing a first flow rate of said audio data generated by said first audio processing module and a second flow rate of said audio data consumed by said second audio processing module when said first clock source is different from said second clock source.

2. The audio system according to Claim 1, wherein:

said first audio processing module comprises an accelerator module; and

said second audio processing module comprises a renderer module.

3. The audio system according to Claim 1, wherein:

said first audio processing module comprises a local stage; and

said second audio processing module comprises a global stage.

4. The audio system according to Claim 1, wherein:

said first audio processing module comprises a first accelerator module; and

said second audio processing module comprises a second accelerator module.

5. The audio system according to Claim 1, wherein:

said first audio processing module comprises a first local stage; and

said second audio processing module comprises a second local stage.

6. The audio system according to Claim 1, wherein:

said first audio processing module is configured to store audio data in a shared portion of said buffer, when said first and second audio processing modules share a common clock source; and

said second audio processing module is configured to retrieve audio data from said shared portion of said buffer, when said first and second audio processing modules share said common clock source.

7. The audio system according to Claim 1, wherein:

said first audio processing module is configured to store said audio data in an input portion of said buffer, when said first and second audio processing modules do not share a common clock source;

said sample rate converter is configured to retrieve said audio data from said input buffer, to modify said audio data by insert or delete an extra sample and to store said

modified audio data in an output portion of said buffer, when said first and second audio processing modules do not share said common clock source; and

said second audio processing module is configured to retrieve said audio data from said output portion of said buffer, when said first and second audio processing modules do not share said common clock source.

8. The audio system according to Claim 1, wherein:

said first audio processing module is configured to store audio data in a shared portion of said buffer, when said first and second audio processing modules do not share a common clock source;

said second audio processing module is configured to retrieve audio data from said shared portion of said buffer, when said first and second audio processing modules do not share said common clock source; and

said sample rate converter is configured to increase a rate of generation by said first audio processing module or decrease a rate of consumption by said second audio processing module, when said first and second audio processing modules do not share said common clock source.

9. The audio system according to Claim 1, wherein:

said first clock source of said first audio processing module is determined from a first global unique identifier of said first audio processing module; and

said second clock source of said second audio processing module is determined from a second global unique identifier of said second audio processing module.

10. A method for synchronizing audio processing modules comprising:

registering a plurality of audio processing modules;

determining if an associated set of audio processing modules utilize a common clock source; and

configuring a first one of said associated set of audio processing modules to pass a first set of audio data through a first buffer to a second one of said associated set of audio processing modules, when said associated set of audio processing modules utilize said common clock source.

11. The method according to Claim 10, further comprising:

configuring said first one of said associated set of audio processing modules to store said first set of audio data in a second buffer, when said associated set of audio processing modules do not utilize said common clock source;

configuring said sample rate converter to receive said first set of audio data from said second buffer, to store a second set of audio data in a third buffer and to synchronize a flow rate of said first set of audio data into said second buffer with a flow rate of said second set of audio data out of said third buffer, when said associated set of audio processing modules do not utilize said common clock source; and

configuring said second one of said associated set of audio processing modules to receive said second set of audio data from said third buffer, when said associated set of audio processing modules do not utilize said common clock source.

12. The method according to Claim 11, wherein said first one of said associated set of audio processing modules generates said first set of audio data as a function of one or more received sounds.

13. The method according to Claim 11, wherein said second one of said associated set of audio processing modules performs:

rendering a playback signal as a function said first set of audio data, when said associated set of audio processing modules utilize said common clock source; and

rendering said playback signal as a function of said second set of audio data, when said associated set of audio processing modules do not utilize said common clock source.

14. The method according to Claim 11, wherein said second one of said associated set of audio processing modules performs:

recording an input signal as a function of said first set of audio data, when said associated set of audio processing modules utilizes said common clock source; and

recording said input signal as a function of said second set of audio data, when said associated set of audio processing modules do not utilize said common clock source.

15. The method according to Claim 11, wherein said first one of said associated set of audio processing modules processes said first set of audio data.

16. The method according to Claim 11, wherein said second one of said associated set of audio processing modules performs:

processing said first set of audio data, when said associated set of audio processing modules utilize said common clock source; and

processing said second set of audio data, when said associated set of audio processing modules do not utilize said common clock source.

17. A method for synchronizing audio processing modules comprising:

operating in a first mode, when an associated set of audio processing modules share a common clock source, comprising;

storing audio data generated by a first one of said associated set of audio processing modules in a shared buffer; and

receiving audio data consumed by a second one of said associated set of audio processing modules from said shared buffer; and

operating in a second mode, when said associated set of audio processing modules do not share a common clock source, comprising;

storing audio data generated by said first one of said associated set of audio processing modules in an input buffer;

receiving audio data consumed by said second one of said associated set of audio processing modules from an output buffer; and

synchronizing a first flow rate of audio data being stored in said input buffer with a second flow rate of audio data being received from said output buffer.

18. The method according to Claim 17, further comprising determining a clock source of each audio processing module.

19. The method according to Claim 18, wherein said determining a clock source of each audio processing module comprises:

polling each audio processing module; and

receiving an identifier of said clock source of each audio processing module.

20. The method according to Claim 17, wherein said synchronizing comprises:

receiving said audio data from said input buffer;

inserting or deleting an extra sample in said audio data to generate modified audio data;

storing said modified audio data in said output buffer.

21. A computing device comprising:

a memory controller hub;

a processor communicatively coupled to said memory controller hub;

a main memory communicatively coupled to said memory controller hub; and

an audio system communicatively coupled to said memory controller hub comprising;

a clock manager;

a plurality of audio processing modules communicatively coupled to said clock manager;

a sample rate converter communicatively coupled to said clock source; and

a buffer communicatively coupled to said plurality of audio processing modules and said sample rate converter.

22. The computing device according to Claim 21, wherein said clock manager and said sample rate converter are implemented by information and instructions stored in said main memory and processed by said processor.

23. The computing device according to Claim 21, wherein at least one of said plurality of audio processing modules are an integral part of said memory controller hub.

24. The computing device according to Claim 21, further comprising an input/output controller hub communicatively coupled to said memory controller hub, wherein at least one of said plurality of audio processing modules are an integral part of said input/output controller hub.

25. The computing device according to Claim 21, wherein said buffer is implemented in said main memory.